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		2-Mar-15	

IBIS Quality Report

Company:	STMicroelectronics
IBIS file name	m24c32_fd1_tssop8.ibs
IBIS Version:	4.0

	IBIS QUALITY REPORT	date	2 (8)
		2-Mar-15	

Contents

1. MODELING..... 3

1.1 Component description..... 3

1.2 Modeling conditions..... 3

1.3 Circuit for data extraction 5

2. IBISCHK6 CHECK 6

2.1 Result Check by IBISCHK6 6

3. FUNCTIONAL CHECK..... 7

3.1 Functional verification..... 7

4. EXTRA INFORMATION 8

	IBIS QUALITY REPORT	date	3 (8)
		2-Mar-15	

1. MODELING

IBIS (I/O, Buffer, Information, Specification) provide a standardized way, officially EIA standard 656-A-1999 and IEC 62014-1, to model behaviorally a digital component input, output and I/O buffers.

1.1 Component description

Component reference	Technology	Component description
M24C32 M24C64 M24128	CMOS F8H+ (P4)	The M24C32/64/128 is a 32/64/128 Kbit I ² C-bus compatible EEPROM (Electrically Erasable PROgrammable Memory) operating with a supply voltage ranging from 1.7V to 5.5V, over the -40°C to 85°C temperature range.

1.2 Modeling conditions

Simulator used	AMS 2010.1 (Mentor Graphics)
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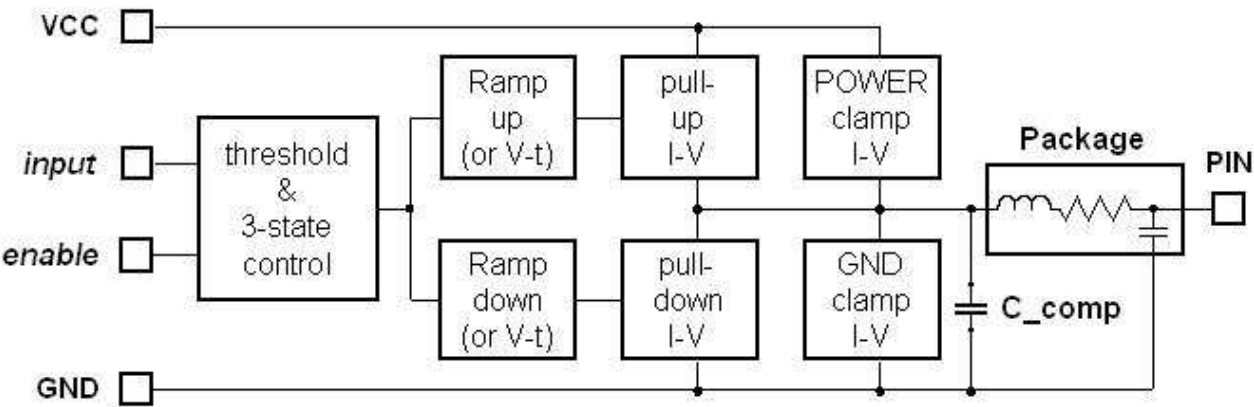


Figure 1: IBIS model generic structure

conditions	Typical	Minimum	Maximum
Temperature [C°]	25	-40	85
Voltage Supply [Volt]	1.8	1.7	2.0
Process setting	nom	weak	strong

	IBIS QUALITY REPORT	date	4 (8)
		2-Mar-15	

Model names (of Component)	Model Type	C_comp (typ, min, max)
mod_sda	I/O_Open_Drain	1.845pF (typ), 1.762pF(min) , 2.023pF (max)
mod_scl	Input	1.763pF (typ), 1.683pF (min) , 1.933pF (max)
mod_wc	Input	1.763pF (typ), 1.683pF (min) , 1.933pF (max)
mod_en	Input	1.763pF (typ), 1.683pF (min) , 1.933pF (max)

Model names (of Component)	Threshold and Vmeas	Timing parameters (if used)
mod_scl/wc/en	Vinl=0.54V , Vih=1.26V	
mod_sda	Vmeas=9.00V	Rref=1k, Cref=10pF, Vref=1.80V

Package	description/comment
TSSOP8	Thin Shrink Small Outline Package 8 leads

	IBIS QUALITY REPORT	date	5 (8)
		2-Mar-15	

1.3 Circuit for data extraction

The I-V data are extracted by simulations using the simulation setup shown in figure 2 below. This model is an I/O model, other model type derived from this structure. For more accurate modeling, certain combinations of V-T tables are recommended (with exception of Input-only model types) using the simulation setup shown in figure 3, with load conditions specified.

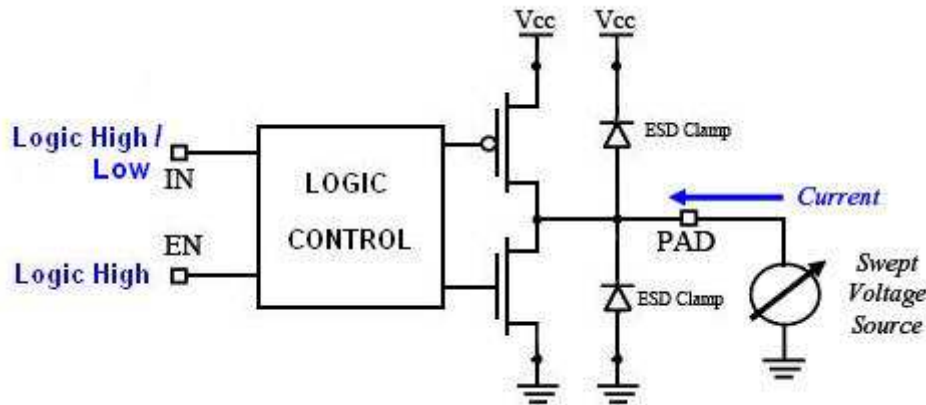


Figure 2: Simulation Setup to extract **I/V** data from I/O model type

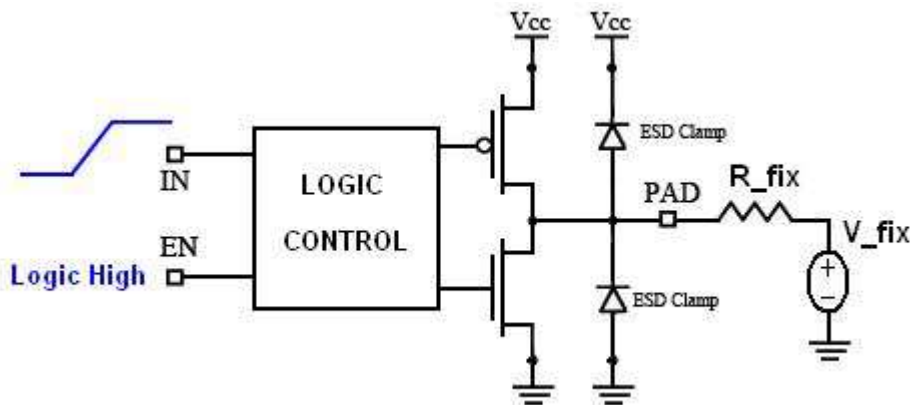


Figure 3: Simulation Setup to extract **V/T** data from I/O model type (see also Table 1)

V/T data condition extractions	Load conditions
Rising waveform	R_fix=50 Ohm, V_fix= 0 V
Rising waveform	R_fix=50 Ohm, V_fix= 1.8 V
Falling waveform	R_fix=50 Ohm, V_fix= 1.8 V
Falling waveform	R_fix=50 Ohm, V_fix= 0 V

Table 1: V/T curve extraction load conditions

	IBIS QUALITY REPORT	date	6 (8)
		2-Mar-15	

2. IBISCHK6 CHECK

The created IBIS model must be checked using IBISCHK5 parser to ensure that the syntax is correct. The result of the check is showed in the next section with some comments (optional).

2.1 Result Check by IBISCHK6

IBISCHK6 V6.0.1

Checking m24c32_fd1_tssop8.ibs for IBIS 4.2 Compatibility...

NOTE (line 293) - Pulldown Typical data is non-monotonic

NOTE (line 293) - Pulldown Minimum data is non-monotonic

NOTE (line 293) - Pulldown Maximum data is non-monotonic

Errors : 0

File Passed

Adding comments about the Warning or Note:
<p>The output check contains some Note about non-monotonic data of I-V curves, but they are not indicative of problems inside the model.</p>

	IBIS QUALITY REPORT	date	7 (8)
		2-Mar-15	

3. FUNCTIONAL CHECK

The created IBIS model must be compared with the Original Buffer circuit. The signal outputs, in the same load conditions (Figure 4), must match. These output comparisons are presented in TYP, MIN and MAX condition. This section cannot be defined for Input and Terminator model type, because they are input-only model types.

How well results are matched?	Put “X” into the right filed
Curves shape match correctly, but there is a little time translation.	
Curves shape match correctly, but there is a mismatch into the Overshoot and/or Undershoot regions.	
Curves match well.	X

3.1 Functional verification

Circuit used for output comparison results is illustrated in figure 4.

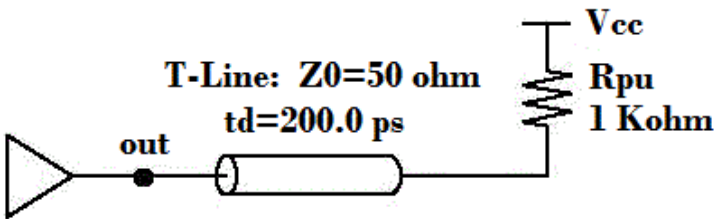


Figure 4: Circuit used for functional check

	IBIS QUALITY REPORT	date	8 (8)
		2-Mar-15	

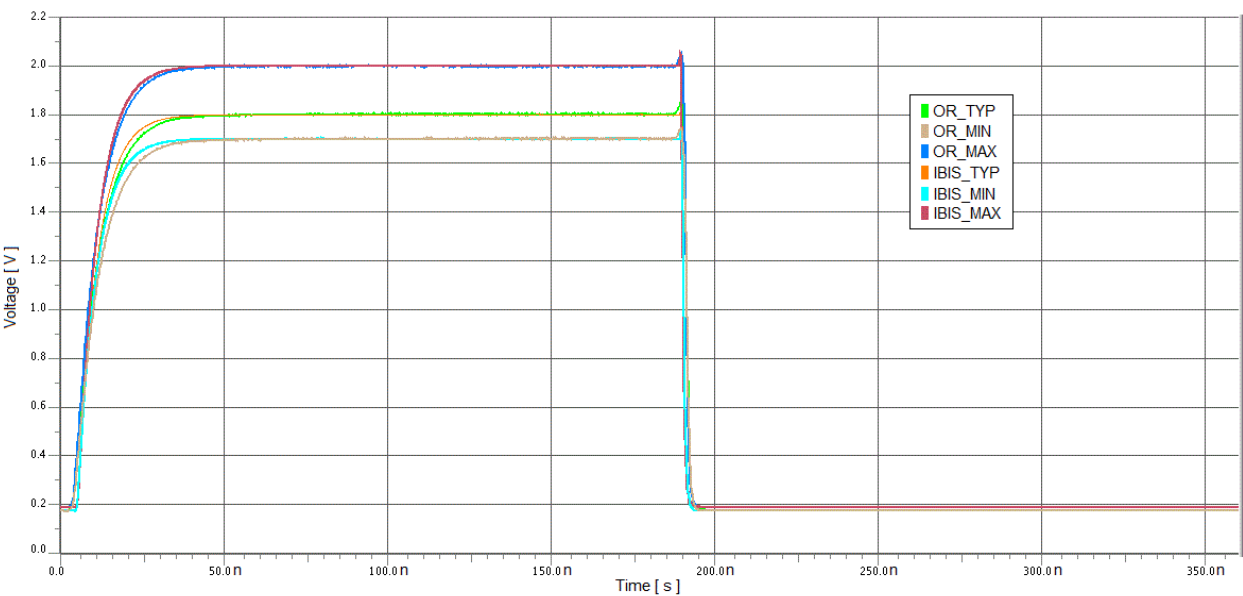


Figure 5: IBIS vs Eldo comparison results of “mod_sda” Model

Output Comparisons:

Adding comments about the comparison:

4. EXTRA INFORMATION

This section can contains other extra informations, to explain some other features of peculiar IBIS model

Other specifications	description